REMARKS

Claims 1-3 and 5-24 remain in this application. Claims 1, 11, 17 and 22 have been amended. Claim 4 has been cancelled. Claims 1, 11, 17 and 22 are independent claims.

In an Office action dated March 23, 2005, all of the pending claims were rejected in view of the prior art. As noted in the Office action, all amendments and arguments were considered. All rejections of claims 1-24 set forth in the first Office action were maintained and the claims were deemed unpatentably distinct over the prior art of record.

Claims 1-4, 9-16 and 22-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. Additionally, claims 4-8 and 17-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. in view of Quach. Applicants have amended claims 1, 11, 17 and 22. Section 714.22 of the MPEP provides that after final rejection amendments may be admitted if (a) the amendments will place the claims in a condition of patentability or in better form for appeal, and (b) upon showing of good and sufficient reason why they are necessary and were not earlier presented.

Applicants believe amendments in response to the first Office action, and remarks made in support for the amendments, placed the claims in a condition for patentability. The second Office action, in rejecting all claims as unpatentable and finding no allowable subject matter, made it necessary for Applicants to amend the claims further in order to place them in a condition of patentability. It is respectfully requested that the proposed amendments to the independent claims be entered and reconsideration be granted.

A. Patentability of Claim 1

Claim 1 has been amended by incorporating subject matter from dependent claim 4 to further clarify the operation of the volatile memory checker described by the claims. The features described in Applicants' claim 4 were rejected as allegedly being taught by Jiang et al. Applicants respectfully point out that Section 2143.03 of the MPEP provides that to establish *prima facie* obviousness, all claim limitations must be taught or suggested by the prior art. In In re Royka, 180 USPQ 580 (CCPA 1974) it was held that all words in a claim must be considered in judging the

patentability of that claim. It is respectfully asserted that the prior art references whether taken alone or in combination do not teach a volatile memory checker that includes a timing module enabled to trigger execution of test code in response to the detection of a passage of a preselected period of time and simultaneous detection that said device is in a period of inactivity, as described in the currently amended claim 1.

The Office action cites that Jiang et al. teaches a timing diagram associated with built-in testing of volatile memory in Figures 7-9. Fig. 7 illustrates the BIST write access. The built-in self-test read access is illustrated in Fig. 8. BIST read invert write cycles are illustrated in Fig. 9. The timing diagrams disclose that a predetermined number of clock cycles must occur in order for the BIST to accomplish its intended function. For instance (col. 7, lines 45-52), the BIST write access requires four clock cycles to complete (Fig. 7). Built-in self-test reads are 16 bit accesses which require two cycles (Fig. 8). A read-invert-write access takes four cycles (Fig. 9). Detection that the required number of clock cycles have passed prior to execution of the next step of the BIST is necessary in order for BIST to operate properly. However, this is not equivalent to the simultaneous detection that the device is in a period of inactivity.

Referring to Fig. 5 (col. 6, lines 37-43) of Jiang et al., the core tests are begun (Step 1999) and the built-in self-test begins by the core test calling it (Step 2000). The BIST may be started by setting the BIST status bits to 0 (Step 2002). The particular tests are begun by setting the appropriate bit in the status/control register BISTSC (Step 2004). There is no teaching or suggestion that the core test has simultaneously detected that the device is in a period of inactivity when setting the BIST status bit at Step 2002 or when beginning a particular test by setting the BISTSC register at step 2004.

Table 7 of Jiang et al. provides definitions for each of the BIST interface signals illustrated in the diagrams. BISTA (14:1) is a BIST address signal. BISTDO (15:0) is a "data write with" signal, and BISTDI (15:1) is a "data read with" signal. The $\overline{BIST}$ and $\overline{BISTRMW}$ are BIST "read" and "read-modify-write" signals, respectively. $\overline{BIST256}$ is BIST access to 256 bits. $\overline{BISTMODE}$ is asserted during the entire BIST. Lastly, the $\overline{IGNORE}$ signal is only used during the pseudo-writes to DRAM. It is asserted that none of these interface signals teaches or discloses detection of the device being in a period of inactivity. The signal diagrams are illustrative of what occurs during the BIST operation, after it has been enabled to Step 2004 (Fig. 5)

or Step 2024 (Fig. 6) and triggered to execute at Step 2006 (Fig. 5) or Step 2026 (Fig. 6) with no determination if the device is in a period of inactivity.

The data retention test, cited by the Office action as a test for soft errors, would be enabled at Step 2024, and once the appropriate control bit had been read, the test would proceed (col. 7, lines 6-8). There is no teaching or suggestion that simultaneous detection that the device is in a period of inactivity occurs when the appropriate bit in the BISTSC status/control register is read and the test enabled to proceed. The predetermined waiting period during which a dummy write to a pseudo address is executed ($\overline{IGNORE}$ signal, Fig. 7) and the subsequent read and compare are taking place during Steps 2030 and 2032, simultaneous detection that the device is in a period of inactivity is not taught or suggested at these steps. When an error is detected, the test is stopped (Steps 2034-2036), but only the test. The BIST remains active and stores the address of the failed memory location to a test register. The BIST then proceeds with the remaining tests, if there are any. It is asserted that there is no teaching in any of the steps of the BIST or timing diagrams disclosed in Jiang et al. of a timing module enabled to trigger execution of test code in response to the detection of a passage of a preselected period of time and simultaneous detection that said device is in a period of inactivity.

The secondary reference to Quach is related to detection of soft errors, but there is no suggestion in either the primary reference to Jiang et al. or the secondary reference to Quach to modify the system of Jiang et al. to more closely approach Applicants' invention, as now claimed. Even if one were to modify Jiang et al. to include the teachings of Quach, the modification would not render the claimed invention unpatentable under Section 103(a), since neither patent teaches or suggests a volatile memory checker having a timing module enabled to trigger execution of test code in response to detection of a passage of a preselected time period and simultaneous detection that a device is in a period of inactivity.

Quach teaches detection of a soft error when the processor is operating the execution cores in redundant mode (col. 2, lines 40-42). The redundant mode (col. 3, lines 41-44) may be a high reliability (HR) processor execution mode that reduces the risk of soft errors when executing critical code segments. Method 300 (col. 8, lines 64-67; col. 9, lines 1-6) is initiated when an error is detected 310 while the processor is operating in redundant mode. When the error is detected 310, the processor jumps to an error

recovery routine (ERR). The ERR switches 330 the processor from redundant mode to split mode. Split mode (col. 3, lines 44-47) may be a high performance processor execution mode that is available to process selected code faster, by increasing the execution resources available to the selected code. The split mode may also be available for only selected purposes, such as error recovery.

Quach, in teaching that a soft error is detected while the process is operating, clearly identifies a device that is in a period of activity. When performing error recovery in split mode, the processor or device in Quach is also in a period of activity. The significant aspect of split mode (col. 3, lines 48-52) is that it allows the execution code to operate "independently," i.e., each may execute different instructions in a given cycle. This suggests that one of the dual processors may perform ERR and the other is executing instructions for operating a device. In addition, there is no teaching that the volatile memory checker in Quach triggers execution of test code in response to detection of a passage of a preselected time period. Moreover, it is reasonable to infer that the volatile memory check in Quach is enabled upon detection that the device is in a period of activity, since the error detection method is initiated to detect errors while the processor is operating.

It is asserted that Quach teaches away from Applicants' amended claim 1. There would be no motivation to modify Jiang et al. in view of Quach because there would be no reasonable expectation of success that the combined references would teach Applicants' invention as currently claimed. It is further asserted that independent claim 1, as amended, is materially different over the prior art reference to Jiang et al. Therefore, it is respectfully asserted that amended independent claim 1 and its dependent claims are in an allowable condition and reconsideration is requested.

B. Patentability of Claim 11

Claim 11 describes the invention as performing time-based volatile memory checking routines in response to detecting that a device is in an inactive state and a preselected time period has elapsed. The patentability of claim 11 based on the above limitations was argued in response to the first Office action. Nevertheless, the claim was rejected in the second Office action.

It is Applicants' assertion that not all limitations of the claim were fully considered as provided for in Section 2143.03 of the MPEP. In addition, the above limitation encompasses subject matter similar to that of independent claim 1, as currently amended. Many of the remarks with regard to the patentability of claim 1 apply equally to the determination of the patentability of claim 11.

However, the second Office action being a final rejection, Applicants find it necessary to amend independent claim 11 in order to overcome the rejection of the second Office action and place the claim in condition for allowance. It is respectfully asserted that the prior art references either alone or in combination do not teach a volatile memory that is susceptible to soft errors, the soft errors being those errors occurring during an inactive state, the inactive state being a passage of time during which the device is idle. Applicants' amended claim 11 clearly describes the device being idle, not merely the volatile memory being idle.

The Office action alleged that it would have been obvious to modify Jiang et al. to test for errors in volatile memory, including data retention errors or soft errors. Jiang et al. defines a data retention test (col. 5, lines 57-59) as a test designed to verify that the DRAM core retains a 1 or a 0 for a duration of time equal to the refresh time period. The data retention test includes (col. 3, lines 26-32) (1) writing a first data background to each memory location, (2) waiting a predetermined period of time during which a dummy write to a pseudo address is written and (3) reading and comparing each memory location to the first data background. The data retention error occurs during a predetermined inactivity period or refresh period of the volatile memory.

Jiang et al. teaches (col. 2, lines 45-47) that the RAM is only a portion of a processing unit also having a CPU and test unit. Even if the waiting of a predetermined period of time were considered an inactive state during which a device is idle, it would only pertain to the refresh period which is specific to the RAM and not the processing unit or device as a whole.

The secondary reference to Quach teaches detection of soft errors (col. 2, lines 40-42) when the processor is operating the execution cores in redundant mode. In redundant mode (col. 4, lines 62-65), execution cores 110 execute the same instructions from a code segment in LOCK step, and the results are compared by check unit 130 to detect errors in either execution core 110. The check unit performs its checks when the processor

is operating and while each execution core is executing the same code segments.

On the other hand, Applicants' invention includes performing volatile memory checking routines in response to detecting that the device is in an inactive state and a preselected time has elapsed. The inactive state is described as a passage of time during which the device is idle. In addition, Applicants' claim describes the soft errors as errors that occur in executable code during the inactive state between execution of executable code. Quach makes no such teaching. Quach merely teaches the cause and effect that encompass a soft error. That is (col. 1, lines 12-14), soft errors arise when alpha particles or cosmic rays strike an integrated circuit and alter the charges stored on the voltage nodes of the circuit. There is no teaching that the charges stored on the voltage nodes are altered during an inactive state, the inactive state being a passage of time during which the device is idle.

Therefore, even if Jiang et al. were modified in view of Quach, the method would not teach checking of memory during a period of time in which the device is idle. Applicants respectfully submit that amended independent claim 11 and its dependent claims are in an allowable condition.

C. Patentability of Claim 17

Amended claim 17 describes an integrated circuit that includes a self-tester being responsive to a time-based test initialization signal for triggering periodic testing, the time-based initialization signal being dependent upon a passage of time intervals related to a time of day. Support for the amendment can be found in Paragraph [0025] of the application as originally filed, wherein the self-testing for soft errors occurs as a function of time. A test initialization module 60 tracks time. Time increments may be based upon a time of day. For example, the self-testing may be initiated once per day at the same time of day or may be initiated once per hour.

Jiang et al. teaches a built-in self-test (BIST) for detecting errors in DRAM. Figs. 7-9 teach that execution of the BIST is related to a passage of time intervals. However, these time intervals are related to cycles of the CLOCKOUTA signal and not to a time of day. There is no teaching in Jiang et al. that the CLOCKOUTA signal may be interpreted or decoded to relate to a time of day. Even if the CLOCKOUTA signal were considered to be a time-based initialization signal for triggering the BIST, it is not equivalent to a

time-based initialization signal dependent upon the passage of time intervals related to a time of day, as described in Applicants' amended claim 17.

The secondary reference, Quach, teaches detection of soft errors while operating in redundant mode. The execution cores execute (col. 4, lines 62-65) the same instructions from a code segment in LOCK step, and the results are compared by check unit 130. There is no teaching in Quach when specifically the test unit 130 is initialized. However, the check unit having to compare the results of the same code segments executed by each execution core, there being no teaching or suggestion in Quach to the contrary, it is reasonable to infer that the check unit is initialized based upon the passage of time intervals related to the execution of the code segments and not a time of day, as described in Applicants' invention.

Even if one were to modify Jiang et al. to include the teachings of Quach, the modification would not render the claimed invention unpatentable under Section 103(a), since neither patent teaches or suggests a time-based initialization signal dependent upon a passage of time intervals related to a time of day.

Therefore, it is respectfully asserted that amended independent claim 17 and its dependent claims are in a condition for allowance.

D. Patentability of Claim 22

Claim 22 describes a system for managing information storage, including storing information within memory that is susceptible to occurrences of soft errors, the memory being within a device that is characterized by extended periods of inactivity between periods of activity, and the extended period of inactivity being passages of time during which said device is idle. The system also includes an automated memory checker configured to execute test code on a timed basis to detect soft errors within the stored information, the timed basis being dependent upon a passage of time intervals related to a time of day.

Remarks made in support of independent claim 11 can be applied in support of claim 22, describing an extended period of inactivity as being a passage of time during which a device is idle. Similarly, remarks made in support of independent claim 17 can be applied in support for claim 22, describing an automated memory checker being configured to

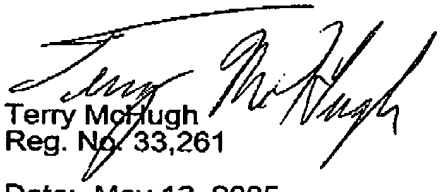
execute test code on a timed basis in which the timed basis is dependent upon a passage of time intervals related to a time of day.

As previously remarked, Jiang et al. teaches detection of data retention errors which occur during a predetermined wait state in which the volatile memory of a device is inactive. Jiang et al. does not teach the device being inactive. Quach teaches detection of soft errors while operating in redundant mode or period of activity, not during a period of inactivity.

Moreover, Jiang et al. teaches a built-in self-test in which the timing of the test operation is related to a passage of time intervals related to the CLOCKOUTA signal. Quach teaches a check unit to detect errors in timing intervals related to the execution of instructions from a code segment. Neither prior art of record teaches an automated memory checker configured to execute test code and timed basis in which the timed basis is dependent upon a passage of time intervals related to a time of day.

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,



Terry McHugh
Reg. No. 33,261

Date: May 13, 2005

Telephone: (650) 969-8458
Facsimile: (650) 969-6216